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EXAMINER	
MAIS, MARK A	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,923	BREWER ET AL.	
	Examiner	Art Unit	
	Mark A Mais	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-53 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-53 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02 March 2001.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 2, 2001 was filed after the mailing date of the Application on December 19, 2000. The submission is in compliance with the provisions of 37 CFR 1.56 and 1.97. Accordingly, the examiner considered the information disclosure statement.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 11-18, 25-26, 35-36, and 43-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Sriram (USP 5,463,620).

4. With regard to claim 1, Sriram discloses a communication network router **[Fig. 3, node 10]** containing an egress queuing structure **[Fig. 6, Queues 1 through *n*]** comprising:

a plurality of substantially parallel queues **[Fig. 6, Queues 1 through *n*]**, each said queue having an input terminal and an output terminal **[Fig. 5, inputs to multiplexer 29 (i.e., to Queues 1 through *n* (of Fig. 6)), include inputs to queues such as voice queue 32 through video delivery queue 46, all of which connect to server 48]**;

a common shared memory device interconnected with all of said plurality of queues **[it is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45]**;

a queue congestion processor interconnected with said input terminals of all of said queues **[Fig. 3, ATM Switch Fabric 25 performs table lookups and processes/distributes packets according to QOS/COS classification, col. 4, lines 59-63]**;

an output selection block interconnected with said output terminals of all of said queues **[Fig. 6, time slice allocator 52 determines and controls how many cells are to be output from each queue during each multiplexing period, col. 8, line 66 to col. 9, line 3]**; and

an egress arbitration processor interconnected with said output selection block **[the output of server 48, specifically, output from the DTS Cell Selection Controller 50, goes to link 28, wherein DTS Cell Selection Controller 50 selectively connects each of queues 1 through n to output link 28, col. 8, lines 62-66]**.

5. With regard to claim 7, Sriram discloses a router further comprising a plurality **[Fig. 3, a plurality of queuing structures stem from multiple output links 26, 28, and 30, wherein each output link 26, 28, and 30 each contain their own queuing structure]** of said egress queuing structure, each said queuing structure **[Fig. 6, Queues 1 through *n*]** comprising:

a plurality of substantially parallel queues **[Fig. 6, Queues 1 through *n*]**, each said queue having an input terminal and an output terminal **[Fig. 5, inputs to multiplexer 29 (i.e., to Queues 1 through *n* (of Fig. 6)), include inputs to queues such as voice queue 32 through video delivery queue 46, all of which connect to server 48]**;

a common shared memory device interconnected with all of said plurality of queues **[it is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45]**;

a queue congestion processor interconnected with said input terminals of all of said queues **[Fig. 3, ATM Switch Fabric 25 performs table lookups and processes/distributes packets according to QOS/COS classification, col. 4, lines 59-63]**;

an output selection block interconnected with said output terminals of all of said queues **[Fig. 6, time slice allocator 52 determines and controls how many cells are to be output from each queue during each multiplexing period, col. 8, line 66 to col. 9, line 3]**; and

an egress arbitration processor interconnected with said output selection block **[the output of server 48, specifically, output from the DTS Cell Selection Controller 50, goes to link 28, wherein DTS Cell Selection Controller 50 selectively connects each of queues 1 through n to output link 28, col. 8, lines 62-66]**.

6. With regard to claim 11, Sriram discloses an egress queue management for a router comprising:

receiving packets having payload pointers **[Fig. 2, interpreted with respect to ATM packets as the 6th octet, or rather, the first octet of information field 13 wherein the payload pointer is well-known with respect to ATM packets]**, packet data payloads **[Fig. 2, information field 13]**, and packet lengths **[each generic ATM packet length is well-known; special packets lengths depending on type of packet, as well as packet lengths with respect to short packets (less than the standard ATM packet length), follow the ATM standards of the CCITT]** into a queuing structure comprising a plurality of queues **[Fig. 6, Queues 1 through *n*]**;

assigning the packets to separate queues in accordance with their quality of service (QOS) priority levels **[Fig. 5, each queue is assigned to one quality of service (e.g., output voice queue 32 through video delivery output queue 46, col. 3, lines 48-49)]**;

storing the packet payload pointers in the queues ;

storing the packet payloads in a common memory pool shared by all of the plurality of queues **[it is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44]**;

releasing said packets from said queues into a common egress tributary using a rate metering mechanism **[examiner interprets rate metering as the allocation of specific bandwidth for each type of QOS accomplished by TDM, col. 5, lines 51-53]**.

7. With regard to claim 35, Sriram discloses an instantaneous queue congestion management of drop probabilities of packets **[examiner interprets drop probabilities management as a table lookup using the traffic tables (bandwidth versus capacity), col. 7, lines 30-36]** using a queue congestion management algorithm **[the pre-allocated bandwidth is expressed through the time slice allocations of the time slice allocator 52 which is proportionate to bandwidth requirements depending the QOS, col. 6, lines 57-62]** applied to a plurality of queues **[Fig. 6, Queues 1 through *n*]** sharing a common memory pool **[it is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44]**.

8. With regard to claims 2 and 8, Sriram discloses that the queue congestion processor is interconnected with an egress reassembly logic **[the virtual channel identifier (VCI) in the ATM header allows the ATM Switch Fabric 25 to perform packet-classification according to the classification table, col. 4, lines 54-63; which examiner interprets as packet reassembly]** .

9. With regard to claims 3 and 9, Sriram discloses that the output selection block is interconnected with a single tributary of a router egress port **[Figs. 3 and 6, output link 28 is one output port of node 10, col. 3, lines 41-42]**.

10. With regard to claim 4, Sriram discloses that each queue is assigned to a single quality of service (QOS) priority level **[Fig. 5, each queue is assigned to one quality of service (e.g., output voice queue 32 through video delivery output queue 46, col. 3, lines 48-49)]**.

11. With regard to claim 5, Sriram discloses that each queue is assigned to a different QOS priority level **[Fig. 5, each queue is assigned to one quality of service (e.g., output voice queue 32 through video delivery output queue 46, col. 3, lines 48-49)]**.

12. With regard to claim 6, Sriram discloses that the plurality of queues are assigned to four different QOS priority levels **[types 1A, 1B, 2 and 3, col. 3, line 61 to col. 4, line 53]**.

13. With regard to claim 12, Sriram discloses that the separate queues are assigned among four different QOS priority levels **[types 1A, 1B, 2 and 3, col. 3, line 61 to col. 4, line 53]**.

14. With regard to claim 13, Sriram discloses that the rate metering mechanism comprises:

pre-allocating a bandwidth for each QOS priority level **[the pre-allocated bandwidth is expressed through the time slice allocations of the time slice allocator 52 which is proportionate to bandwidth requirements depending the QOS, col. 6, lines 57-62]**;

periodically adding tokens to a counter associated with each said QOS priority level queue, such that the tokens are added to each counter at a time averaged rate substantially proportional to the pre-allocated bandwidth of the QOS priority level; and applying a rate metering algorithm to said queues**[Fig. 7, the flowchart shows that for each QOS-specific queue *i*, a counter is used to determine that the *m* allocated cells are output from queue *i* onto output 28 at a time-averaged rate until the time-slice period is over or until the queue is empty, col. 9, lines 26-43]**.

15. With regard to claim 14, Sriram discloses setting maximum and minimum limits on the number of tokens in the counter **[inherently, there is a minimum and maximum amount of time that a queue *i* can empty it's allotted packets depending on the allocated time slice for that specific queue and the time-averaged *m* cells output from queue *i*]**.

16. With regard to claim 15, Sriram discloses that the rate metering algorithm is implemented in hardware **[it is inherent that the rate metering can be done in either software or hardware]**.

17. With regard to claim 16, Sriram discloses that the rate metering algorithm comprises:

for each QOS priority level queue in sequence, starting with the highest QOS priority level, if there is a packet in the queue and if there are positive tokens in the counter associated with the queue, then releasing a packet from the queue **[Fig. 7, the flowchart shows that for each QOS-specific queue *i*, a counter is used to determine that the *m* allocated cells are output from queue *i* onto output 28 at a time-averaged rate until the time-slice period is over or until the queue is empty, col. 9, lines 26-43]**; otherwise

for each QOS priority level queue in sequence, starting with the highest QOS priority level, if there is a packet in the queue, then releasing a packet from the queue regardless of whether tokens are in the counter **[users, and therefore queues, are guaranteed the requested peak bandwidth for the duration of the call and therefore, reserved, col. 7, lines 18-21;]**; and

for each packet released from a queue, deducting a number of tokens from the counter associated with the queue in proportion to the size of the packet **[Fig. 7, the flowchart shows that for each QOS-specific queue *i*, a counter is used to determine that the *m* allocated cells are output from queue *i* onto output 28 at a time-averaged rate until the time-slice period is over or until the queue is empty, col. 9, lines 26-43]**;.

18. With regard to claim 17, Sriram discloses instantaneous queue congestion management of drop probabilities of the packets using a queue congestion management algorithm before assigning the packets to the queues **[calls involving statistically multiplexed services are admitted when permitted to do so in light of information contained in traffic tables stored in the node (depending on number of calls and bandwidth required), col. 2, lines 21-26]**.

19. With regard to claim 18, Sriram discloses that the queue congestion management algorithm is implemented in hardware **[it is inherent that the statistically multiplexing can be accomplished in either software or hardware]**.

20. With regard to claims 25 and 43, Sriram discloses that the queue congestion management algorithm comprises:

determining the total amount of shared memory space in bytes **[inherently determined or already known]**; monitoring the instantaneous actual sizes of each of said queues **[when performing statistical multiplexing, the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23]**

dynamically calculating minimum and maximum queue sizes of a drop probability curve for each of the queues **[inherently, there is a minimum and maximum queue size calculated depending on the QOS or class of service already-partitioned-out; especially since the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23]**;

comparing said instantaneous actual sizes with the maximum and minimum queue sizes **[examiner interprets such comparison as a table lookup using the traffic tables (bandwidth versus capacity), col. 7, lines 30-36]**;

if the instantaneous queue size is less than the minimum queue size, then assigning the packet to the queue **[the pre-allocated bandwidth is expressed through the time slice allocations of the time slice allocator 52 which is proportionate to bandwidth requirements depending the QOS, col. 6, lines 57-62]**;

otherwise if said instantaneous queue size is between the maximum and minimum queue sizes, then calculating and applying a drop probability using the slope of said drop probability curve **[examiner interprets such comparison as a table lookup using the traffic tables (bandwidth versus capacity), col. 7, lines 30-36]**; and otherwise

if said instantaneous queue size is greater than said maximum queue size, then dropping the packet **[when performing statistical multiplexing, the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23, if the packet is not admitted, it is considered 'dropped']**.

21. With regard to claims 26 and 44, Sriram discloses that non-utilized shared memory space is allocated simultaneously **[unused bandwidth, and, therefore, memory space, is allocated temporarily to all other potential traffic in the system with a priority on higher QOS, col. 7, lines 45-48]** to all of the queues sharing the common memory pool **[it is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44]**.

22. With regard to claim 36, Sriram discloses that the queue congestion management algorithm is implemented in hardware **[it is inherent that the congestion management algorithm can be done in either software or hardware]**.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram as applied to claims 1-9 above.

25. With regard to claim 10, Sriram does not specifically disclose that plurality of tributaries are interconnected with a single router egress port **[Figs. 3 and 6, output link 28 is one output port of node 10, col. 3, lines 41-42]**. Examiner takes Official Notice that multiple switch fabrics can be output through one switch/router output port. Multiple outputs from multiple switch fabrics provide better and faster switching capability/capacity for packets that are input to the router/switch. Moreover, switch fabric architecture can be constructed as one discrete NxM fabric or a series of smaller switch fabrics that provide the same functionality. However, a many-discrete-switch fabric has to deal with bandwidth, arbitration, and contention control; and is one of the reasons for making one larger NxM fabric. It would have been obvious to one of ordinary skill in the art at the time of the invention to use several discrete switch fabrics or a larger switch fabric in order to design an invention that includes the NxM switching function depending on the needs, needed capabilities/capacity, and aesthetics of the invention. For example, Ofek (USP 6,674,754) discloses the use of multiple switching fabrics that are fed into one output port [Fig. 1, multiple switching fabrics 50 are fed into one output port 1 40].

26. Claims 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram as applied to claims 11-17 above.

27. With respect to claims 19-24, Sriram does not specifically disclose the use of a floating-point format. However, the statistical multiplexing can be accomplished with either the traffic tables stored in the node or in real-time using a statistical algorithm. Examiner takes Official Notice that statistical algorithms can use one of several formats to include a floating-point format. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a floating-point format for applying the statistical math formula using a processor. For example, Brooks et al. (USP 6,151,615) discloses the use of a floating-point format that uses mantissa table lookup. Moreover, Applicants have not disclosed that a specific type of floating-point format arrangement to include a 4-bit rounded (normalized) mantissa, a 6-bit biased exponent, a mantissa table with two 3-bit inputs and a 4-bit output, and using only positive numbers solves any stated problem or is for any particular purpose. It appears that the performance of the statistical multiplexing would result equally well with the traffic tables disclosed in Sriram. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the traffic tables of Sriram to use another statistical multiplexing methodology such a s a floating point format because such a modification is considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Sriram. In addition, using a specific length/value mantissa and exponent is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. *See* In re Aller, 105 USPQ 233 (CCPA 1955).

28. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram as applied to claim 11 above, further in view of Random Early Detection Gateways for Congestion Avoidance (RED Gateways) (Sally Floyd and Van Jacobson, Random Early Detection Gateways for Congestion Avoidance, August 1993, IEEE/ACM Transactions on Networking, Abstract).

29. With respect to claim 27, Sriram discloses a time averaged congestion management of drop probabilities of the packets before assigning the packets to the queues or dropping the packets **[when performing statistical multiplexing, the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23, if the packet is not admitted, it is 'dropped']** as applied to the queues having different QOS priority levels and sharing a common memory pool **[it is obvious, and therefore, examiner takes Official Notice that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, it would have also been obvious to implement one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44]**.

Sriram does not specifically disclose using a weighted random early discard (WRED) algorithm applied to the queues having different QOS priority levels. RED Gateways discloses the use of a weighted random early discard making use of statistical multiplexing based on probabilities. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted the statistical multiplexing of Sriram (**table lookup using the traffic tables (bandwidth versus capacity), col. 7, lines 30-36)** with the WRED statistical multiplexing disclosed in RED Gateways **[Abstract]** in order to keep the average queuing-size-per-QOS low and to control the size depending on the bandwidth allocated to the particular queue **[*see Id.*]**.

30. With respect to claim 28, Sriram discloses that the WRED algorithm is implemented in hardware **[Examiner takes Official Notice that it is obvious to implement an algorithm in hardware. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the algorithm in either software or hardware]**.

31. Claims 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram further in view of RED Gateways, as applied to claims 27-28 above.

32. With respect to claims 29-34, neither Sriram nor RED Gateways specifically discloses the use of a floating-point format. However, the statistical multiplexing can be accomplished with either the traffic tables stored in the node or in real-time using a statistical algorithm such as RED Gateways. Examiner takes Official Notice that statistical algorithms can use one of several

formats to include a floating-point format. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a floating-point format for applying the statistical math formula using a processor. For example, Brooks et al. (USP 6,151,615) discloses the use of a floating-point format that uses mantissa table lookup. Moreover, Applicants have not disclosed that a specific type of floating-point format arrangement to include a 4-bit rounded (normalized) mantissa, a 6-bit biased exponent, a mantissa table with two 3-bit inputs and a 4-bit output, and using only positive numbers solves any stated problem or is for any particular purpose. It appears that the performance of the statistical multiplexing would result equally well with the traffic tables disclosed in Sriram. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the traffic tables of Sriram to use another statistical multiplexing methodology such a s a floating point format because such a modification is considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Sriram. In addition, using a specific length/value mantissa and exponent is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. *See* In re Aller, 105 USPQ 233 (CCPA 1955).

33. Claims 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram, as applied to claims 35-36 above.

34. With respect to claims 37-42, Sriram does not specifically disclose the use of a floating-point format. However, the statistical multiplexing can be accomplished with either the traffic tables stored in the node or in real-time using a statistical algorithm. Examiner takes Official

Notice that statistical algorithms can use one of several formats to include a floating-point format. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a floating-point format for applying the statistical math formula using a processor. For example, Brooks et al. (USP 6,151,615) discloses the use of a floating-point format that uses mantissa table lookup. Moreover, Applicants have not disclosed that a specific type of floating-point format arrangement to include a 4-bit rounded (normalized) mantissa, a 6-bit biased exponent, a mantissa table with two 3-bit inputs and a 4-bit output, and using only positive numbers solves any stated problem or is for any particular purpose. It appears that the performance of the statistical multiplexing would result equally well with the traffic tables disclosed in Sriram. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the traffic tables of Sriram to use another statistical multiplexing methodology such a s a floating point format because such a modification is considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Sriram. In addition, using a specific length/value mantissa and exponent is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. *See* In re Aller, 105 USPQ 233 (CCPA 1955).

36. Claims 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram further in view of RED Gateways.

37. With regard to claims 45-46, Sriram discloses a time averaged congestion management of drop probabilities of **[when performing statistical multiplexing, the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23, if the packet is not admitted, it is 'dropped']** packets before assigning the packets or dropping them to one of an array of queues having a common memory pool **[it is obvious, and therefore, examiner takes Official Notice that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig. 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, it would have also been obvious to implement one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44]**

Sriram does not specifically disclose using a weighted random early discard (WRED) algorithm applied to the queues having different QOS priority levels. RED Gateways discloses the use of a weighted random early discard making use of statistical multiplexing based on probabilities. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted the statistical multiplexing of Sriram **(table lookup using the traffic tables (bandwidth versus capacity), col. 7, lines 30-36)** with the WRED statistical multiplexing disclosed in RED Gateways **[Abstract]** in order to keep the average queuing-size-per-QOS low and to control the size depending on the bandwidth allocated to the particular queue [***see Id.***].

38. With respect to claim 47, Sriram discloses that the WRED algorithm is implemented in hardware **[Examiner takes Official Notice that it is obvious to implement an algorithm in hardware. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the algorithm in either software or hardware]**.

39. Claims 48-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram further in view of RED Gateways, as applied to claims 45-47 above.

40. With respect to claims 48-53, neither Sriram nor RED Gateways specifically discloses the use of a floating-point format. However, the statistical multiplexing can be accomplished with either the traffic tables stored in the node or in real-time using a statistical algorithm such as RED Gateways. Examiner takes Official Notice that statistical algorithms can use one of several

formats to include a floating-point format. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a floating-point format for applying the statistical math formula using a processor. For example, Brooks et al. (USP 6,151,615) discloses the use of a floating-point format that uses mantissa table lookup. Moreover, Applicants have not disclosed that a specific type of floating-point format arrangement to include a 4-bit rounded (normalized) mantissa, a 6-bit biased exponent, a mantissa table with two 3-bit inputs and a 4-bit output, and using only positive numbers solves any stated problem or is for any particular purpose. It appears that the performance of the statistical multiplexing would result equally well with the traffic tables disclosed in Sriram. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the traffic tables of Sriram to use another statistical multiplexing methodology such a s a floating point format because such a modification is considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Sriram. In addition, using a specific length/value mantissa and exponent is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. *See* In re Aller, 105 USPQ 233 (CCPA 1955).

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Aatresh (USP 6,067,301), Method and Apparatus for forwarding packets for a plurality of contending queues to an output.

(b) Kadambi et al. (USP 6,707,818), Network Switch Memory Interface Configuration.

(c) Ofek (USP 6,674,754), Wavelength division multiplexing combined with time division multiplexing using a common time reference.

(d) Brooks et al. (USP 6,151,615), Method and apparatus for formatting an intermediate result for parallel normalization and rounding technique for floating point arithmetic operations.

(e) Caldera et al. (USP 5,978,359), Allocated and dynamic switch flow control.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A Mais whose telephone number is (571) 272-3138. The examiner can normally be reached on 8:00-4:30.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (703) 305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 6, 2004